FPGA Implementation of behavioral Models for RF Power Amplifiers

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Abstract. This paper presents experimental results of Power Amplifiers modeling controlled in Matlab environment. The model is implemented firstly through VHDL in Hardware and improved then by DSP Builder, this emulation is made in FPGA DSP Development Kit, Cyclone® III Edition-ALTERA proving a proper behavioral modeling for RF or high frequency applications. The whole system is able to consider the memory depth and nonlinearity order based on real PA measurements; this work leaves the option for future implementations as Digital Predistortion as linearization technique of PA behavior. The obtained VHDL results are based on a MPM, compared with DSP Builder and an ANN is trained showing a proper behavior.

Keywords: ANN, FPGA, GUI, Memory, Power Amplifier, VHDL.

1 Introduction

Nowadays, wireless communications scenario demands higher data-rate transmissions, complex envelop techniques like wide code division multiple access (WCDMA) and orthogonal frequency division multiplexing (OFDM) techniques are employed because of their high spectral efficiency, should be noted that to achieve this high data rata transmissions the schemes impose strict linearity requirements.
The Power Amplifier (PA) as the main device in the transmission chain involves undesirable effects as memory and plays a role in the transmitter nonlinearities creation, due that behavioral models have been proposed to represent PAs [1-2]. The PA modeling used for very high frequency (VHF) became an important issue before the fabrication, especially if the undesirable effects are considered for wideband applications in order to predict unexpected results, examples include techniques based on polynomial models trying to reproduce real PA measurements, others taking into account memory depth and nonlinearity order [3-4].

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Volterra Series formalism is a proper and well known technique where the memory depth and nonlinearity order can be considered during the amplification process [5]. However, the nonlinearity is an inherent property of PAs, leading not only to inband signal distortion but also to outband spectral regrowth, which are strictly regulated especially with the current wireless communication systems which are continuously growing.

PAs exhibit memory effects as well, which mean the current output is stimulated by not only the input current but also by the previous input states, based on this affirmation a special truncation as Memory Polynomial Model (MPM) is used in this paper and compared with a model based on Artificial Neural Network (ANN)

The aim of this work is addressed to model and create a link between a software system as Matlab and hardware implementation through Very High Speed Integrated Circuit Hardware Description Language (VHDL) demonstrating a fully PA digital behavior leaving the alternative for a further linearization stage or specific application into Very High Frequency (VHF) band.

Modern Field Programmable Gate Array (FPGA) devices offer a multitude of resources. The FPGA characteristic is the possibility of implementing algorithms directly into hardware, maintaining the parallelism of the functioning in the implementation and thus minimizing the execution time, several implementations in the field are related to FPGA devices offering advantages like reprogrammation, tolerance and debugging errors, reducing nonrecurring engineering cost and shorter processing time [6-8]. In this context, behavioral models implemented in hardware have been explored even for dual band and modern transmission standards as LTE [9-11]. This work shows flexibility between the modeling based on VHDL and DSP Builder through MPM and ANN as modeling technique.

This paper is organized as follows. First in Section 2 the description of the Volterra Series, MPM and ANN are presented. The Section 3 shows the results for the implementation made for MPM and ANN. Finally the Section 4 the conclusions are summarized.

2 Description

2.1 Memory Polynomial Model

The MPM is a subset of the Volterra series, it consists of several delay taps and nonlinear static functions; and it represents a truncation of the general Volterra series where only the diagonal terms in the Volterra kernels are considered [9]. Thus, the number of parameters is significantly reduced compared to the original series.

The Volterra Series can be defined in discrete domain as equation (1), they can be used to describe the input-output relation considering the undesirable effects as memory:

$$y(n) = \sum_{m_1=0}^{M} h_1(m)x(n-m) + \cdots + \sum_{m_1=0}^{M}\sum_{m_2=0}^{M} h_2(m_1,m_2)x(n-m_1)x(n-m_2) + \cdots + \sum_{m_1=0}^{M}\sum_{m_2=0}^{M}\sum_{m_3=0}^{M} h_2(m_1,m_2,m_3)x(n-m_1)x(n-m_2)x(n-m_3) \quad (1)$$

where $x(n)$ is the complex input base-band signal, $y(n)$ is the complex output base-band signal, h_k are complex valued parameters and M is the memory depth. The MPM can be represented in equation (2):

$$y(n) = \sum_{q=0}^{Q} \sum_{k=1}^{K} a_{2k-1} |x(n-q)|^{2(k-1)} x(n-q) \quad (2)$$

where $a_{k,q}$ are complex valued parameters, Q is the memory depth, and K is the polynomial order. Equation (2) can be rewritten just in terms of the memory depth, by the following equation (3):

$$y(n) = \sum_{q=0}^{Q} F_q(n-q) = F_0(n) + F_1(n-1) + F_2(n-2) + \ldots + F_q(n-q) + \ldots + F_Q(n-Q) \quad (3)$$

where $F_q(n)$ can be expressed as equation (4) :

$$F_q(n) = \sum_{k=1}^{K} a_{2k-1} |x(n-q)|^{2(k-1)} x(n) \quad (4)$$

Each MPM stage can be subdivided in terms of the desired memory depth during the modeling; this can be represented in Fig. 1 showing the internal structure and the delays made for each step of the input signal. Each stage can be subdivided by internal processes related to the nonlinearity order where the calculated constants must be inserted. In Fig. 2 the internal stage for each delay is represented.

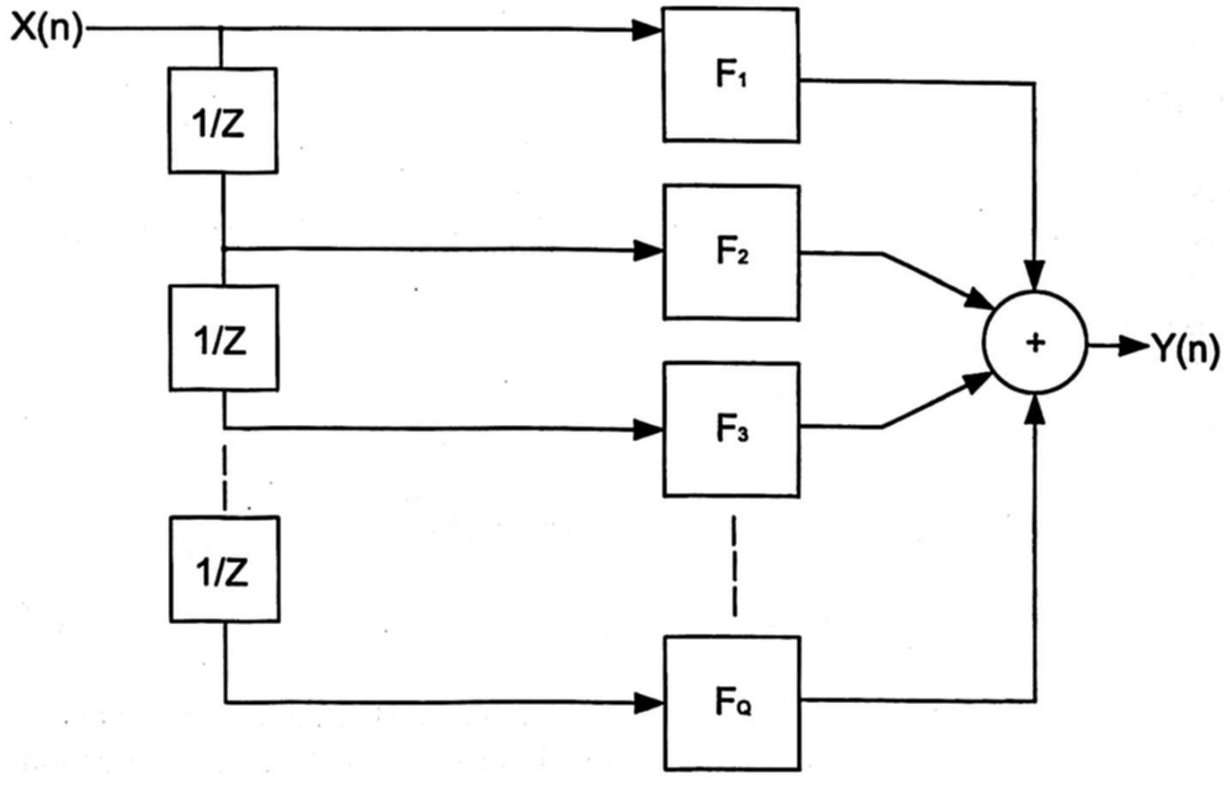


Fig. 1. General structure of the MPM

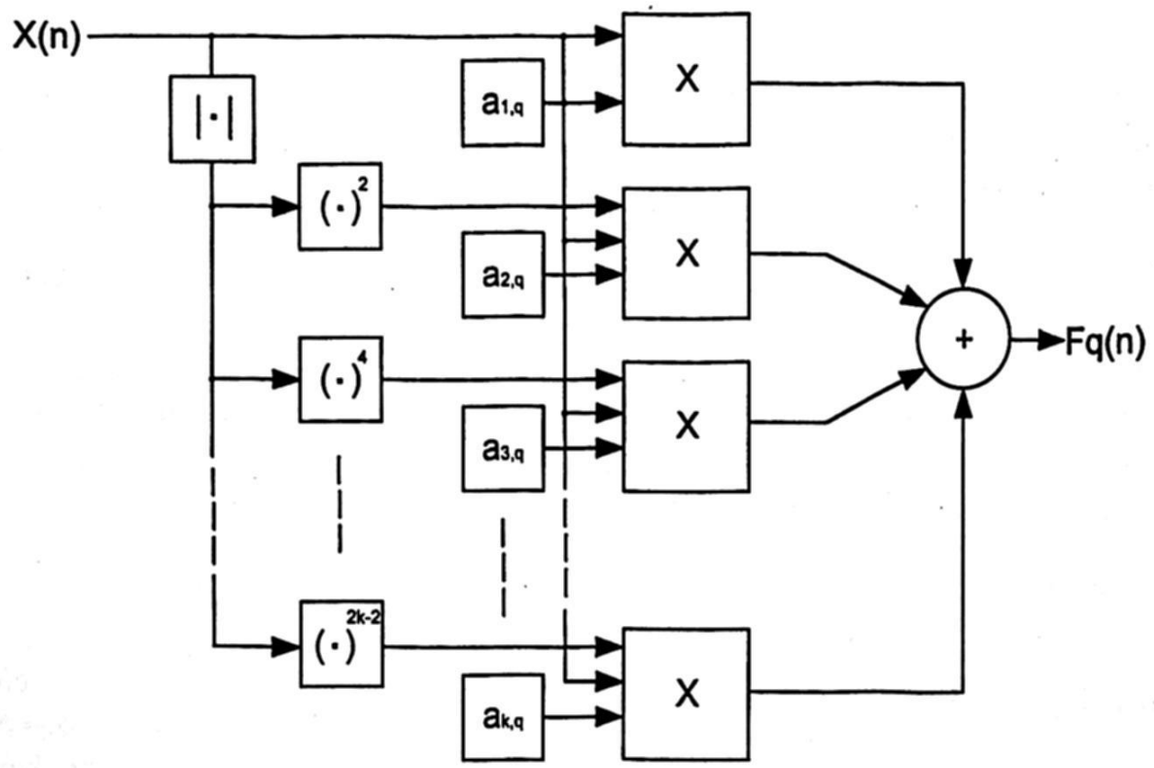


Fig. 2. Internal structure of each stage of the MPM.

The modeling based on MPM can be reproduced through ANN, this work makes use of its advantages containing five neurons, should be noted that the accuracy can be improved if more neuron are added.

2.2 Artificial Neural Network

A neuron is an element based on a biological model. It consists in a system with input signals with a unique output. The artificial neuron structure can be observed in Fig. 3. Fig. 4 represents an ANN where the weights can be denoted by *w(i,j)* and a propagation law is expressed by the equation (5):

$$h_i(t) = \sigma\left(w_{ij}, x_j(t)\right); h_i(t) = \sum w_{ij} x_j \tag{5}$$

The activation function can be denoted in the equation (6):

$$y_i(t) = f_i(h_i(t)) \tag{6}$$

Based on the biological model, the neuron has a threshold θ. The inputs summatory is multiplied by its weight and the activated neuron has a response denoted by equation (7).

$$y(t) = f\left(\sum_j^n w_{ij} x_j - \theta_i\right) \tag{7}$$

$$y_i = 1, si\ \sum_j^n (w_{ij}x_j) > \theta_i\ o\ 0, si\ \sum_j^n (w_{ij}x_j) < \theta_i \quad (8)$$

A neuron is an information-processing unit that is fundamental to the operation of a neural network. The Fig. 3 shows the model of a neuron, which forms the basis for designing neural networks.

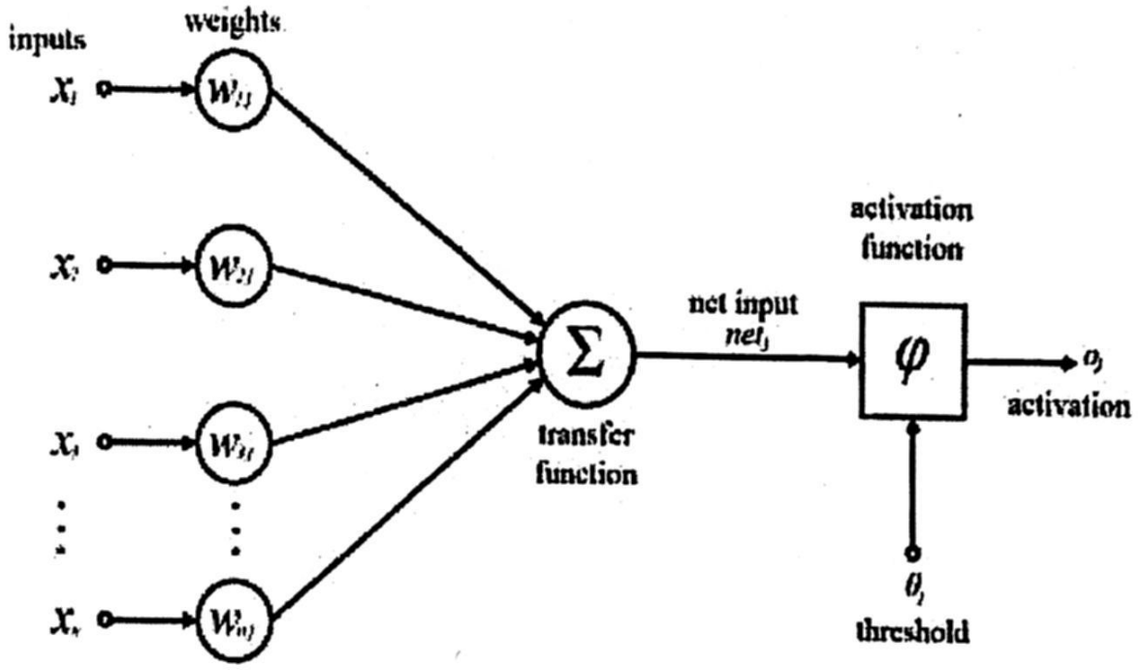


Fig. 3. Overview of a ANN.

Using just a neuron cannot be enough accurate, even more if the system is involving multiple inputs. Associating some neurons as a network, allows an easier emulation of complex functions. Fig. 4 is a representation of an ANN, is said to be fully connected in the sense that every node in each layer of the network is connected to every other node in the adjacent forward layer.

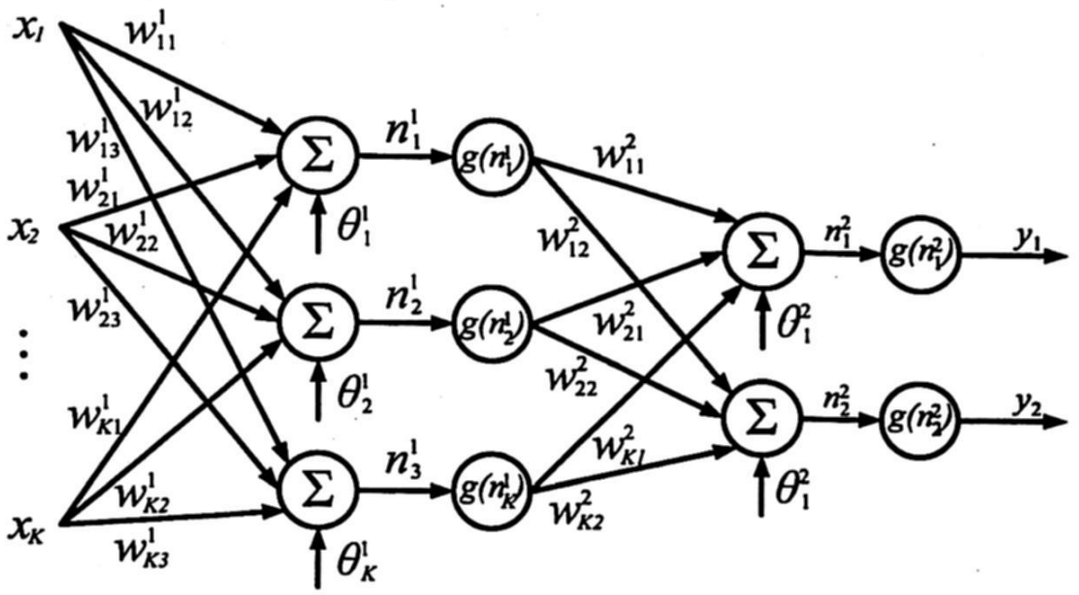


Fig. 4. Representation of an Artificial Neural Network.

ANN has the ability to learn based on an example, making themselves very flexible and powerful for modeling nonlinearity order and memory effect. Furthermore, it has

the capability to learn a complex nonlinear behavior of the dynamic system without the need to understand the internal mechanisms of the system and can be an alternative and attractive approach for PA modeling with memory effects.

2.2.1 The Multilayer Perceptron (MLP)

The simpler architecture is constituted by one input layer, one hidden layer containing a given number of neurons and an output layer. The transfer function of all the neuron is tangent sigmoid type given by the following equation (9):

$$f(x) = \frac{1 - e^{-2x}}{1 + e^{-2x}} \tag{9}$$

The transfer equation of the MLP with one single input layer is quite easy to formulize in equation (10):

$$y = \sum_{k=1}^{K} w_{kj} y_k = \sum_{k=1}^{K} w_{kj} f\left(\sum_{j=1}^{J} w_{ji} x_i\right) \tag{10}$$

Where J is the number of neurons in the hidden layer and K the number of output neurons. The MLP generally uses the back propagation algorithm that consists in actualizing the parameters of the output layer first, then the parameters of the last hidden layer and so. The back propagation algorithm is generally coupled with the Levenberg-Maquart algorithm. This algorithm consists in applying a second derivative to the cost function E to find the maximum gradient.

3 FPGA Implementation

VHDL code is used in electronic design automation to describe digital and mixed-signal systems such as DSP and integrated circuits. The DSP Development Kit Cyclone III Edition-Altera delivers a complete digital signal processing development environment; it includes the Cyclone III development board and Quartus II development software. The system operates with an internal clock of 125 MHz provided by a Phase-Locked Loop (PLL) circuitry. The overall view through blocks of the whole system is showed in Fig. 5.

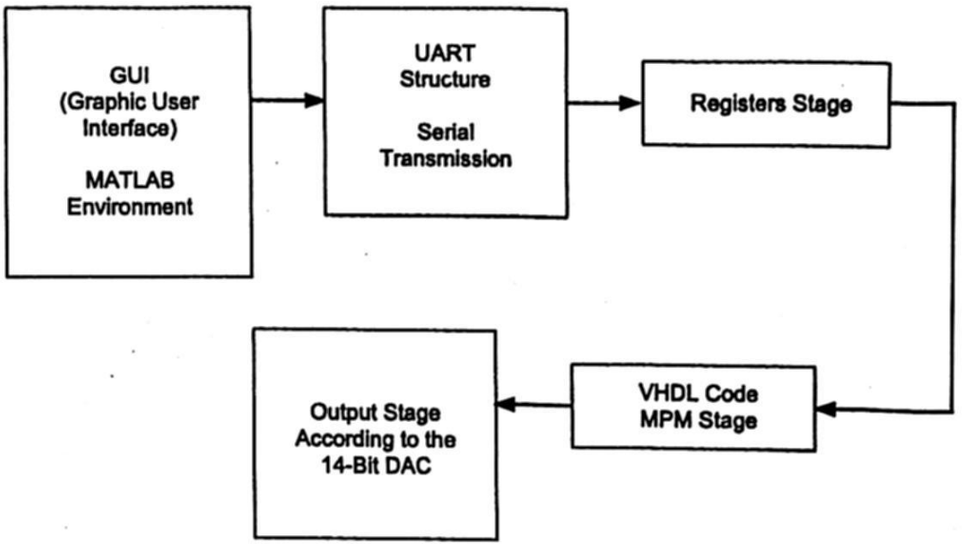


Fig. 5. Block view of the developed VHDL system.

The modeling based on VHDL can be accurate, unfortunately the required code and translation of the MPM coefficients to VHDL environment requires design time.
This Universal Asynchronous Receiver-Transmitter (UART) showed by the VHDL Register-Transfer Level (RTL) is exhibited. In Fig. 6 the UART structure is able to manipulate until 128 calculated records obtained from the workspace in Matlab. There is an internal function in Matlab able to calculate the MPM coefficients based on the LSE technique.
Fig. 7 shows synchronization based on D-Flip Flops during the modeling stage of the send data from Matlab. All these registers are controlled by the same clock provided by the internal clock with frequency 125 MHz.

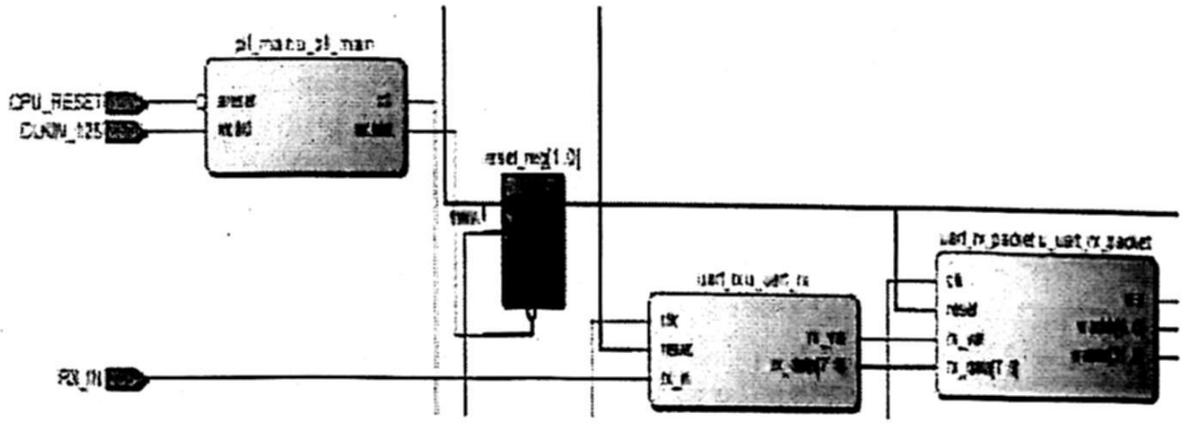


Fig. 6. UART-RTL provided by the Quartus II- ALTERA Software.

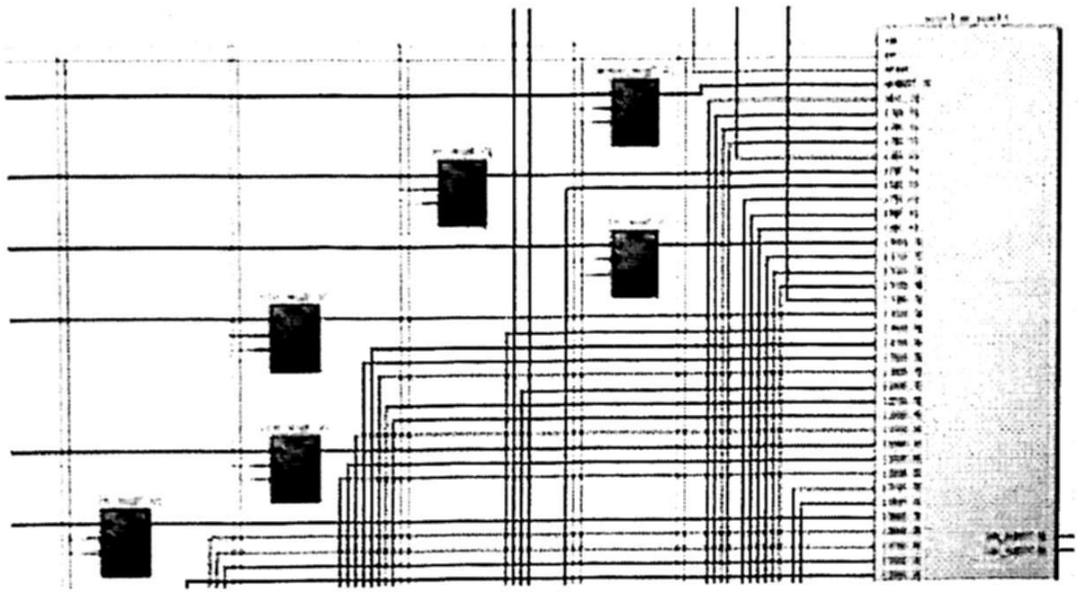


Fig. 7. Coefficients stored as registers and inserted into the Amplification Stage.

In this paper was used the DSP Builder Tool as a faster alternative to run the behavioral modeling. DSP Builder includes basic FPGA block models and enables to build and verify the user's digital system with real hardware parameters without requiring FPGA implementation in the system. Once the system was built, the gencrated outputs are tested by transferring them to the FPGA and emulated them to ensure that they provide similar performance to the MATLAB implementation. Morcover, these high level synthesis tools are able to translate to RTL code directly via an automated process.
The developed system based on DSP Builder is shown in Fig. 8.

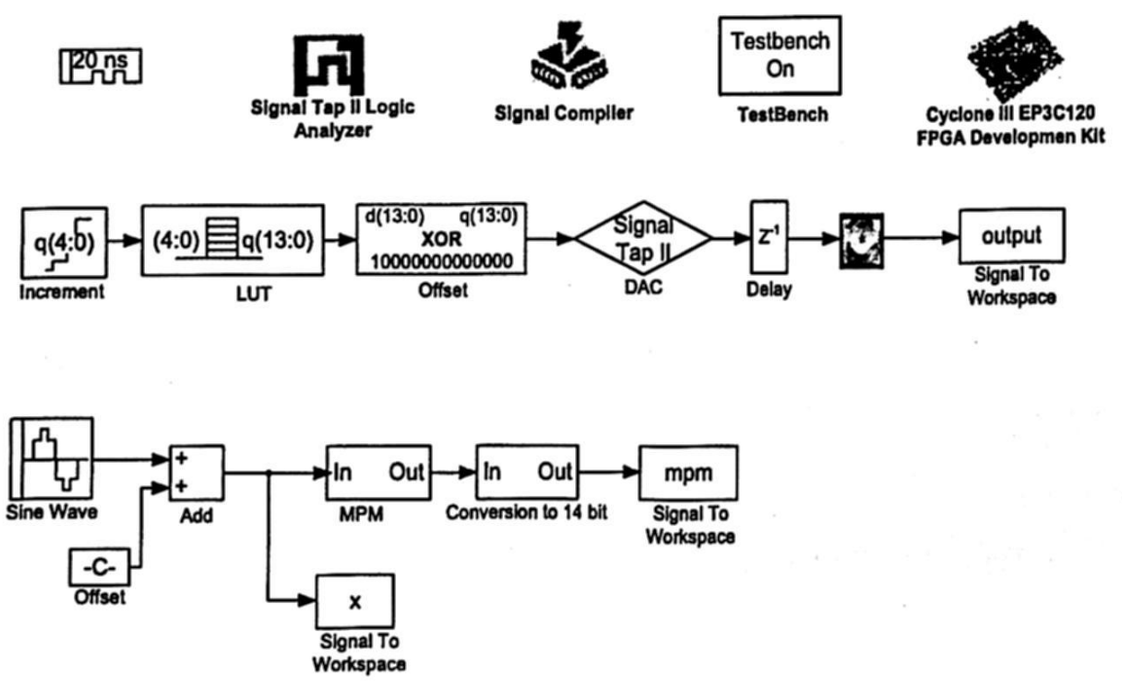


Fig. 8. Overview of MPM implemented using DSP Builder.

The experimental verification of the MPM allows representing any real PAs measurements which closely resembles a real PA behavior. The MPM is exploited during the ANN training including 5 neurons is depicted in Fig. 9.

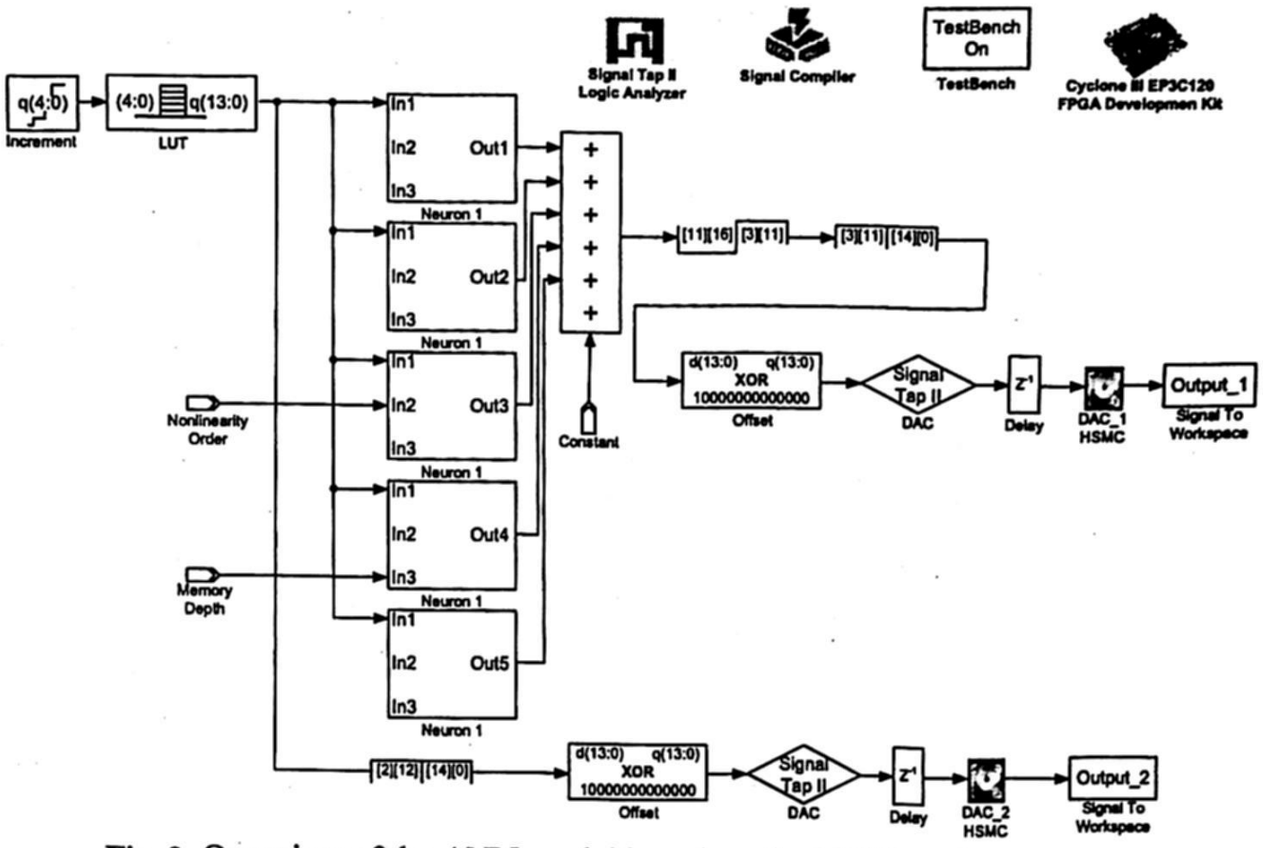
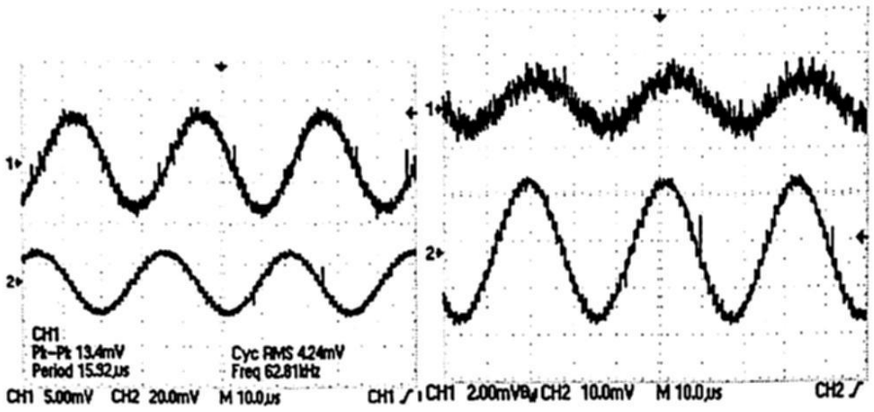


Fig. 9. Overview of the ANN model based on the MPM performance.

4 Results

Fig. 10a shows amplification without memory effects and considering a basic nonlinearity order. In Fig. 10b the memory effects that can be considered for linearization stage are observed, these both results can be achieved through VHDL or DSP Builder. The first part is representing a system with nonlinearity order $n=1$ and memory depth $m=0$, should be noted that the DAC is bounded due to the 14-Bit resolution, for a practical application a power stage must be added in order to increase the signal level and protect the High Speed Mezzanine Card HSMC. The second part shows the modeled output for an input signal with memory depth $m=1$, it can be noted the undesirable memory effect attenuates the output signal. The last emulation depicted in Fig. 11 in hardware was created for a signal with nonlinearity order $n=4$ reaching an output frequency of 1.53 MHz represented in Fig. 11:the sampling frequency was set to 125 MHz.



(a) (b)

Fig. 10. MPM emulated in hardware for a system with (a) nonlinearity order $n=1$ and memory depth $m=0$ and (b) nonlinearity order $n=1$ and memory depth $m=1$.

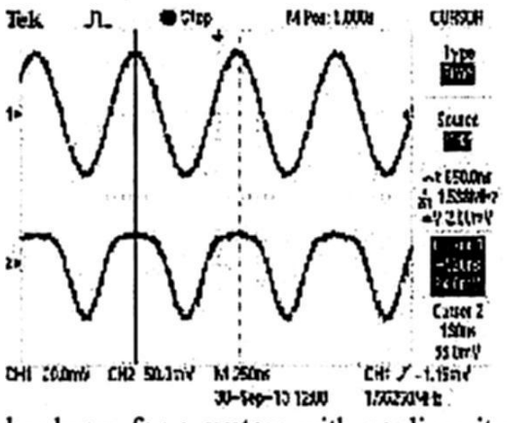


Fig. 11. MPM emulated in hardware for a system with nonlinearity order $n=4$ and memory depth $m=0$.

The modeling for the signal without memory and nonlinearity order $n=1$ has a frequency of 33 KHz, the output frequency can be defined through the sequence and processing in the internal iterations and the desired resolution for each case, this affirmation was done for the case with memory depth $m=1$ and nonlinearity order $n=1$.

5 Conclusion

In this paper, a behavioral modeling based on a special case of Volterra Series modeled with Matlab environment and emulated in Hardware through VHDL using the ALTERA Cyclone III FPGA was presented. The goals of this work have been successfully achieved and show clearly the undesirable effects as memory and nonlinearity order representing closely a real PA behavior. Throughout the project, lots of research regarding modeling PA devices has been gained, all this knowledge can be applied when dealing with nano-devices fabrication when the intermodulation products and memory effects must be considered or they are monitored for a linearization stage. The sampling rate must be considered based on the development board; in this case

the reached frequency of 1.53 MHz was established based on the available development board. The maximum frequency of the signal has to be theoretically 2 times considering the Nyquist sampling criterion, but practically 10 times lower than the frequency of the internal clock established in 125 MHz. This developed work based on VHDL and improved by the DSP Builder tool provides significant advantage related to flexibility and integration about modeling with memory effects, even additional kind of modeling can be added to the system.

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